ACM/IEEE International Conference on Formal Methods and Models for Codesign

MemoCODE

July 26-28, 2010, Grenoble, France

Welcome to the eighth ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2010). The MEMOCODE conference series attracts researchers and practitioners who create methods, tools, and architectures for the design of hardware/software systems. These systems face increasing design complexity including tighter constraints on timing, power, costs, and reliability. MEMOCODE presents novel formal methods and design techniques addressing these issues to create, refine, and verify hardware/software systems.

http://www.memocode-conference.com

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Memocode 2010 Program (1 of 3)

Day 1 (July 26)

8:00 **Registration**

9:00 **Welcome**

9:15 **Invited Talk: Systematic Testing for Control Applications**
Chair: Klaus Schneider, University of Kaiserslautern

Rupak Majumdar, University of California, Los Angeles, California and MPI Saarbrucken/Kaiserslautern, Germany

10:15 **Coffee Break**

11:00 Session 1: Design and Design Methodologies
Chair: Franjo Ivancic, NEC Laboratories

Nirav Dave, Man Cheuk Ng, Michael Pellauer and Arvind. *Modular Refinement and Unit Testing*

David Greaves and Satnam Singh. *Designing Application Specific Circuits with Concurrent C# Programs*

12:00 **Lunch**

13:45 **Session 2: Verification Techniques**
Chair: Viktor Kuncak, EPFL

Bryan Brady, Randal E. Bryant, Sanjit A. Seshia and John O'Leary. *ATLAS: Automatic Term-Level Abstraction of RTL Designs*

Roberto Bruttomesso, Edgar Pek and Natasha Sharygina. *A Flexible Schema for Generating Explanations in Lazy Theory Propagation*

Franjo Ivancic, Malay K. Ganai, Sriram Sankaranarayanan and Aarti Gupta. *Numerical Stability Analysis of Floating-Point Computations Using Software Model Checking*

Tevfik Bultan, Fang Yu and Aysu Betin Can. *Modular Verification of Synchronization with Reentrant Locks*

15:45 **Coffee Break**

16:15 **Design Contest and Poster Presentations**
Chair: Joel Emer, Intel/MIT

Presentations of the design contest winners

19:00 **Reception**

Memocode 2010 Program (2 of 3)

Day 2 (July 27)

9:00 **Invited Talk: The many-cores opportunity for consumer System On Chip.**
Chair: Yassine Lacknech, UJF/VERIMAG

Eric Flamand, STMicroelectronics, Grenoble, France

10:00 **Coffee Break**

10:30 **Session 3: Verification Methods for SystemC**
Chair: Nicola Bombieri, University of Verona

Luca Ferro and Laurence Pierre. *Enhancing the Assertion-Based Verification of TLM Designs with Reentrancy*

Daniel Grosse, Hoang M. Le and Rolf Drechsler. *Proving Transaction and System-level Properties of Untimed SystemC TLM Designs*

Deian Tabakov and Moshe Vardi. *Monitoring Temporal SystemC Properties*

12:00 **Lunch**

14:00 **Tutorial: Formal Verification Methods in Low Power Design Flows**
Chair: Alain Girault, INRIA
Josef Haid, Infineon Technologies, Graz, Austria

15:30 **Coffee Break**

16:00 **Tutorial: Understanding Loops: the Influence of the Decomposition of Karp, Miller, and Winograd**
Chair: Alain Girault, INRIA
Alain Darte, CNRS Laboratoire de l'Informatique du Parallelisme, Lyon, France

17:30 **Panel Discussion: Low Power HW/SW Design: from Technology to Verification**
Chair: Alain Girault, INRIA

20:00 **Banquet**

Memocode 2010 Program (3 of 3)

Day 3 (July 28)

9:00 **Invited Talk: Elastic Circuits**
Chair: Luca Carloni, Columbia University

Jordi Cortadella, Universitat Politecnica de Catalunya, Barcelona, Spain

10:00 **Coffee Break**

10:30 **Session 4: Design Languages**
Chair: Arvind, MIT

Sidharta Andalam, Partha Roop and Alain Girault. *Predictable Multithreading of Embedded Applications Using PRET-C*

Emil Axelsson, Koen Claessen, Gergely Devai, Zoltan Horvath, Karin Keijzer, Bo Lyckgard, Anders Persson, Mary Sheeran, Josef Svenningsson and Andras Vajda. *Feldspar: A Domain Specific Language for Digital Signal Processing algorithms*

Patrick Meredith, Michael Katelman, Jose Mesegeur and Grigore Rosu. *A Formal Executable Semantics of Verilog*

12:00 **Lunch**

13:00 **Session 5: Model Transformations and Transformation Validation**
Chair: Roberto Bruttomesso, University of Lugano

Bin Xue, Sandeep Shukla and Sekharipuram Ravi. *Minimizing Back Pressure for Latency Insensitive System Synthesis*

Julio Peralta, Thierry Gautier and Loic Besnard. *LTSs for Translation Validation of (multi-clocked) Signal specifications*

Mike Gemuende, Jens Brandt and Klaus Schneider. *Compilation of Imperative Synchronous Programs with Refined Clocks*

14:30 **End of Conference**